In re Patent Application of
LIARDET ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**

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connected to the processor and to the multiplexer to receive the scrambling bits from the processor or from a memory.

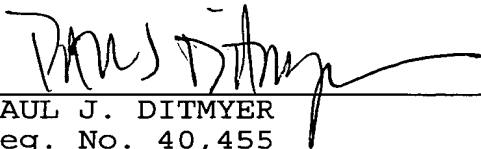32. A method according to Claim 30, wherein the scrambling bits are transmitted randomly.

33. A method according to Claim 30, wherein the scrambling bits are transmitted to the scrambling register whenever key data is input into the plurality of input/output registers.

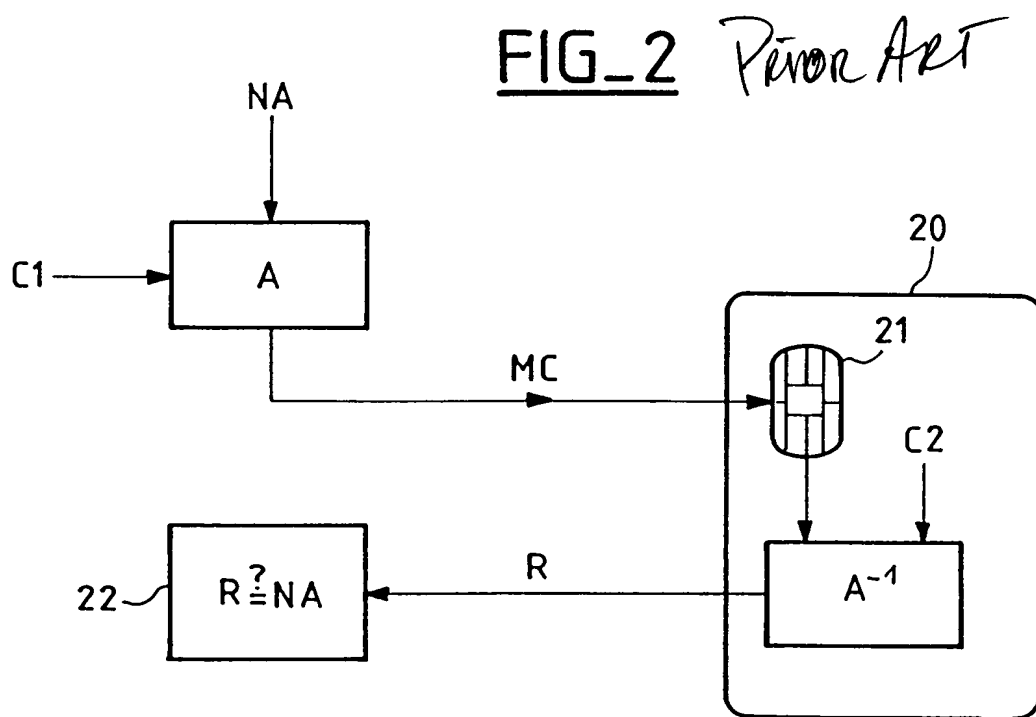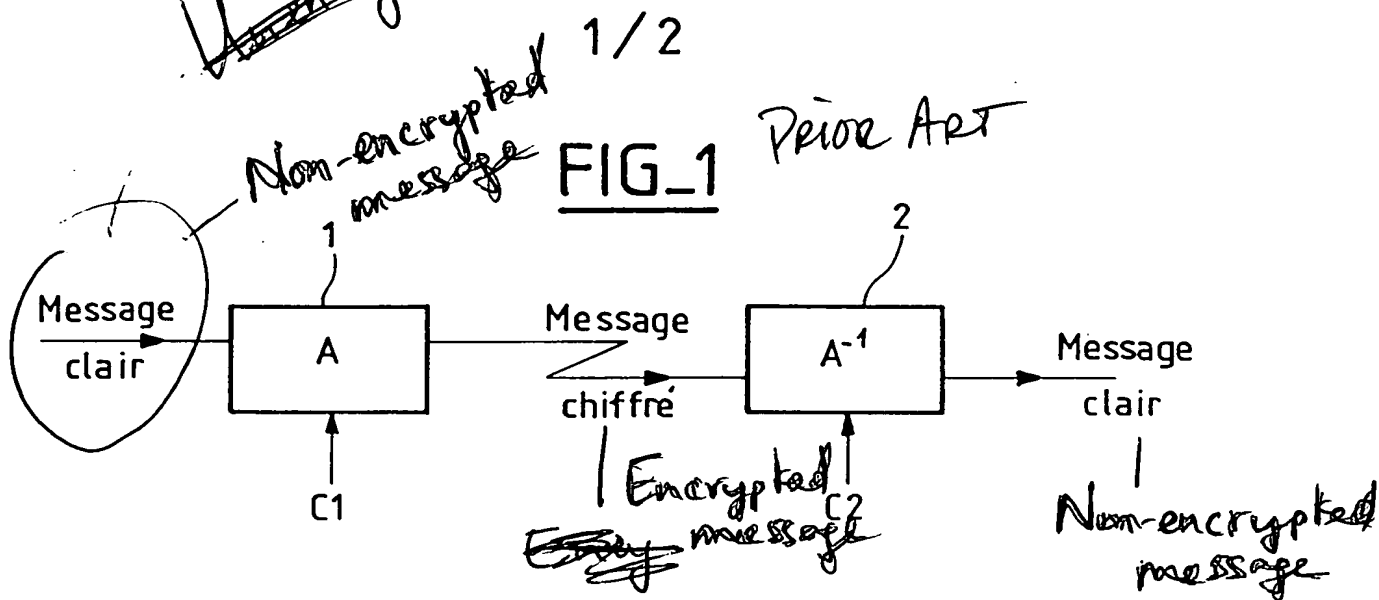34. A method according to Claim 30, wherein the scrambling bits comprise groups of eight bits.

REMARKS

It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.
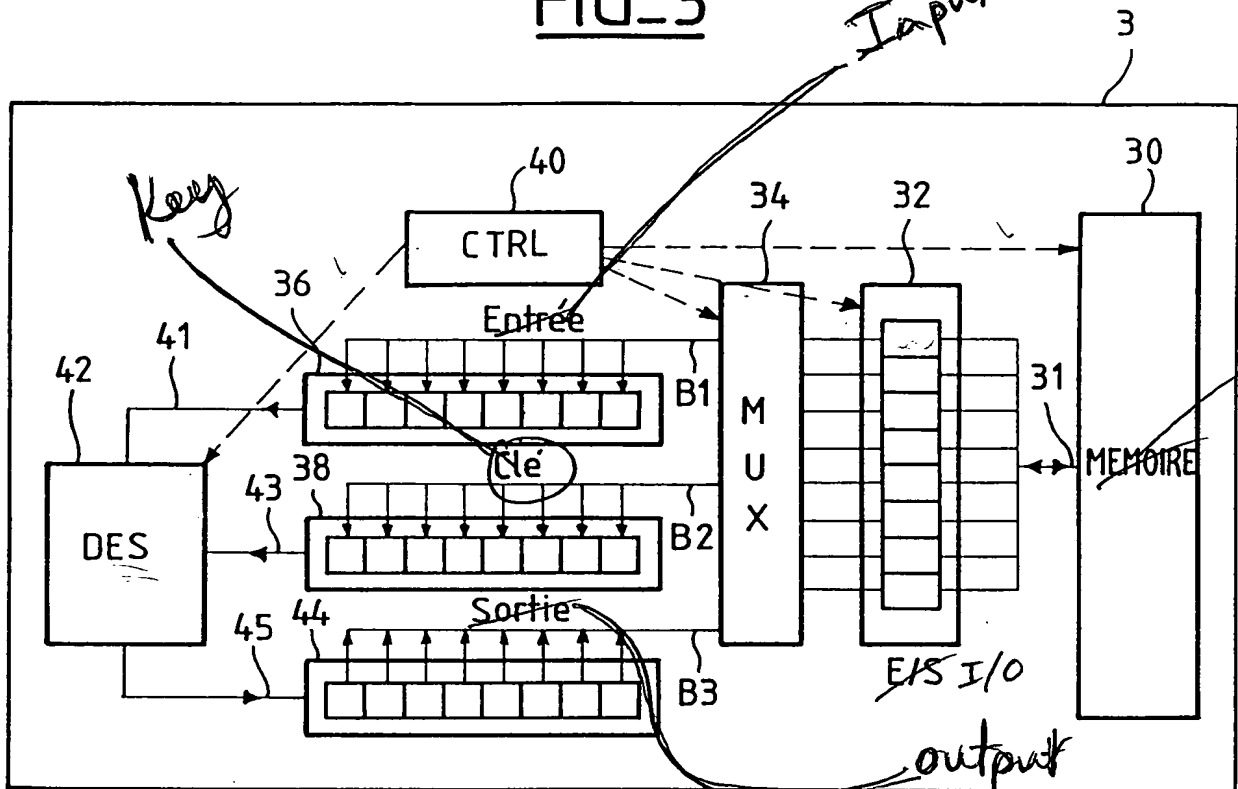
Respectfully submitted,

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FIG_1 Prior Art

Non-encrypted message

Message clair → A → Message chiffré → A^{-1} → Message clair

C1

C2

Encrypted message

Non-encrypted message

FIG_2 Prior Art

NA

C1 → A

MC → 20

21

C2

R → A^{-1}

22 — $R \stackrel{?}{=} NA$

PRIOR ART

Input

FIG_3

- 40 CTRL
- 3
- 34
- 32
- 30
- 36
- Entrée
- Key
- 42 DES
- 41
- B1
- Clé
- 43
- 38
- B2
- M U X
- 31
- MEMOIRE
- Memory
- 45
- 44
- Sortie
- B3
- E/S I/O
- output

FIG_4

- 40 CTRL
- Input
- 50
- 4
- 30
- 58
- 54
- 56
- 52
- 36
- Entrée
- B1
- Key
- 41
- B2
- Clé
- 38
- DES
- 43
- B3
- M U X
- 31
- MEMOIRE
- Memory
- 42
- 45
- 44
- Sortie
- 34
- E/S
- 32
- Output
- I/o